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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/821,531	ALI ET AL.	
	Examiner	Art Unit	
	RuiMeng Hu	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed on 06/09/2009 have been fully considered but they are not persuasive.

Claim 1 recites outputting the frequency specific signal on a single output without additional switching.

Claim 8 recites outputting the frequency modified signal on a single output without the frequency modified signal passing through a switch as part of the outputting.

Claim 14 recites wherein an additional switch is not present after the frequency modification device.

Claim 22 recites an output configured to output the frequency modified signal such that a switch is not located between the frequency modification device and the output.

Applicant argues that the applied references fail to disclose the above newly amended limitations.

The Examiner respectfully submits that Applicant fails to clearly recite there is no switch between the previously mentioned switch and the single output, there is no switch after the single output, and there is no switch after the previously mentioned switch to generate the frequency specific signal on a single output, as to be different from the prior art references.

Regarding **claim 1**, Hjipieris et al. disclose in figure 2, the output of switch 46 is a single output which outputting the frequency specific signal without additional switching, in view of that there is no additional switching after switch 46.

Kapetanic et al. disclose a frequency modification device 96 in figure 1, the output of switch 106 is a single output outputting the frequency specific signal without additional switching, *in view of that the frequency modification device 96 including switch 106, and there is no additional switching after switch 106.*

Regarding **claim 8**, Hjipieris et al. disclose in figure 2, the output of switch 46 is a single output outputting the frequency modified signal without the frequency modified signal passing through a switch as part of the outputting, in view of that there is no additional switching after switch 46.

Kapetanic et al. disclose a frequency modification device 96 in figure 1, the output of switch 106 is a single output outputting the frequency modified signal without the frequency modified signal passing through a switch as part of the outputting, *in view*

of that the frequency modification device 96 including switch 106, and there is no additional switching after switch 106.

Regarding **claim 14**, Hjipieris et al. disclose in figure 2, the output of switch 46 is a single output, wherein an additional switch is not present after the frequency modification device, in view of that the frequency modification device including switch 46.

Kapetanic et al. disclose a frequency modification device 96 in figure 1, the output of switch 106 is a single output, wherein an additional switch is not present after the frequency modification device 96, *in view of that the frequency modification device 96 including switch 106, and there is no additional switching after switch 106.*

Regarding **claim 22**, Hjipieris et al. disclose in figure 2, the output of switch 46 is configured to output the frequency modified signal such that a switch is not located between the frequency modification device and the output, in view of that the frequency modification device including switch 46.

Kapetanic et al. disclose a frequency modification device 96 in figure 1, the output of switch 106 is configured to output the frequency modified signal such that a switch is not located between the frequency modification device 96 and the output, *in view of that the frequency modification device 96 including switch 106, and there is no additional switching after switch 106.*

Response to Amendment

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. **Claim 1** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In claim 1, "a switch" is mentioned twice on lines 13 and 15, it is unclear that whether one or two switches are involved.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1, 8, 14 and 22** are rejected under 35 U.S.C. 102(b) as being anticipated by **Hjipieris et al. (US Patent 5237291).**

Consider **claim 1**, Hjipieris et al. disclose in figure 2, a method for rapidly generating a signal at an output frequency for use in a communication device comprising: providing a reference signal (3MHz reference signal) at a reference frequency to a first signal synthesizer (synthesizer 37 loop 51) configured to generate a first signal at a first frequency; generating the first signal (output of 57) with the first signal synthesizer; processing the first signal to reduce harmonic cross-coupling thereby creating a processed first signal (by filter 59); providing the reference signal (3MHz reference signal) at the reference frequency to a second signal synthesizer (synthesizer

37 loop 53) configured to generate a second signal at a second frequency (output of 61); generating the second signal (output of 61) with the second signal synthesizer; processing the second signal to reduce harmonic cross-coupling thereby creating a processed second signal (by filter 63); providing the processed first signal and the processed second signal to a switch 38; responsive to a control signal (inherently existed); selectively switching a switch 38 to output from the switch 38 either the processed first signal or the processed second signal to create a switch 38 output signal; and after switching either the processed first signal or the processed second signal from the switch 38 and for every switching by the switch 38, shifting (41 or 43) the frequency of the switch 38 output signal to thereby generate a frequency specific signal at a different frequency (output of 46); outputting the frequency specific signal on a single output without additional switching (output of 46).

The same argument applies to claims 8, 14 and 22.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. **Claims 1-13** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Takenouchi et al. (JP 06-338793)** in view of **Kapetanic et al. (US Patent 6163223) and Hjipieris et al. (US Patent 5237291).**

Consider **claim 1**, Takenouchi et al. clearly disclose a method for rapidly generating a signal at an output frequency for use in a communication device comprising (paragraph 1): providing a reference signal (drawing 1, reference signal oscillator 31) at a reference frequency to a first signal synthesizer (drawing 1, PLL 52) configured to generate a first signal at a first frequency; generating the first signal (drawing 1, output of VCO 38) with the first signal synthesizer; providing the reference signal at the reference frequency to a second signal synthesizer (drawing 1, PLL 53) configured to generate a second signal at a second frequency; generating the second

signal (drawing 1, output of VCO 39) with the second signal synthesizer; providing the processed first signal and the processed second signal to a switch (drawing 1, switch 42); responsive to a control signal, selectively switching a switch to output from the switch either the processed first signal or the processed second signal to create a switch output signal; outputting the switch output signal on a single output (paragraph 22).

However Takenouchi et al. fail to specifically disclose processing the first signal to reduce harmonic cross-coupling thereby creating a processed first signal; and processing the second signal to reduce harmonic cross-coupling thereby creating a processed second signal. Such teaching is well known in the art.

In the same field of endeavor, Hjipieris et al. disclose filters for removing unwanted harmonics from a generated oscillating signal wherein processing the first signal to reduce harmonic cross-coupling thereby creating a processed first signal; and processing the second signal to reduce harmonic cross-coupling thereby creating a processed second signal (figure 1, filters 17, 15 and 13, column 2 lines 27-40); shifting (41 or 43) the frequency of the switch 38 output signal to thereby generate a frequency specific signal at a different frequency (output of 46); outputting the frequency specific signal on a single output without additional switching (output of 46).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Hjipieris et al. into the art of Takenouchi et al. as to include the filters for removing unwanted harmonic cross coupling.

However Takenouchi et al. fail to disclose responsive to a control signal, selectively dividing, multiplying, or shifting the frequency of the signal output from the switch to thereby generate a frequency specific signal. Such teaching is well known in the art.

In the same field of endeavor, Kapetanic et al. clearly disclose after switching either the processed first signal or the processed second signal from the switch and for every switching by the switch, shifting the frequency of the switch output signal to thereby generate a frequency specific signal at a different frequency; outputting the frequency specific signal on a single output without additional switching (when switch 10 switches, frequency modifiers 80 and 96 re-adjust themselves to achieve a new specific frequency, column 6 line 65-column 7 line 53, column 8 lines 15-43; figure 1, switch 10, frequency changer 96, column 6 line 65-column 7 line 18).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Kapetanic et al. into the art of Takenouchi et al. as to include controllable frequency modifying means for providing further dynamic frequency control.

Consider **claim 2 as applied to claim 1**, Takenouchi et al. as modified disclose wherein the first signal synthesizer and the second signal synthesizer comprises phase locked loops or delay locked loops (drawing 1, PLL 32, PLL 33).

Consider **claim 3 as applied to claim 1**, Takenouchi et al. as modified disclose wherein processing the first signal and the second signal to reduce harmonic cross-coupling comprises limit or buffer processing (drawing 1, the first or the second PLL

acts as a limiting function, thus a high speed of switching channel is made, as to reduce cross-coupling).

Consider **claim 4 as applied to claim 3**, Takenouchi et al. as modified disclose limiter or buffer processing comprises converting a sinusoidal signal to a signal more closely resembling a square wave signal.

Such converting method is extremely well known in the art (**Tahernia et al. (US Patent 4896122,** figure 3, column 5 lines 54-66).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Tahernia et al. into the art of Takenouchi et al. as modified as to include controllable frequency modifying means for providing further dynamic frequency control.

Consider **claim 5 as applied to claim 1**, Takenouchi et al. as modified disclose wherein dividing, multiplying, or shifting comprises modifying the frequency of the signal output from the switch in proportion to the ratio of the output frequency to either the first frequency or the second frequency (Kapetanic et al. figure 1, switch 10, frequency changer 96, column 6 line 65-column 7 line 18).

Consider **claim 6 as applied to claim 1**, Takenouchi et al. as modified disclose further comprising one or more additional signal synthesizers configured to generate one or more additional signals at one or more additional frequencies (paragraph 10, to choose the output of said two or more-circuit PLL frequency synthesizer circuits).

Consider **claim 7 as applied to claim 1**, Takenouchi et al. as modified disclose wherein the first signal synthesizer and the second signal synthesizer generate signals

at frequencies in addition to the first frequency and the second frequency (said two or more-circuit PLL frequency synthesizer circuits provide multiple different frequency signals based on the CPU control).

Consider **claim 8**, Takenouchi et al. clearly disclose a method for generating an output signal at one or more output frequencies comprising (paragraph 22): generating a first signal at a first frequency (figure 1, output of VCO 38); generating a second signal at a second frequency (figure 1, output of VCO 39); providing the one or more processed output signals to a switch (figure 1, SW 42); selectively outputting based on switch operation at least one processed output signal, and outputting the selected signal (figure 1, CPU controls SW 42 to output the selected signal, paragraphs 25 and 26).

However Takenouchi et al. fail to disclose Limiting processing at least one of the first signal and the second signal to reduce cross coupling to generate one or more limit processed output signals.

In the same field of endeavor, Hjipieris et al. disclose filters for removing unwanted harmonics from a generated oscillating signal wherein processing the first signal to reduce harmonic cross-coupling thereby creating a processed first signal; and processing the second signal to reduce harmonic cross-coupling thereby creating a processed second signal (figure 1, filters 17, 15 and 13, column 2 lines 27-40).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Hjipieris et al. into the art of Takenouchi et al. as to include the filters for removing unwanted harmonic cross coupling.

However Takenouchi et al. fail to disclose selectively modifying the frequency of the signal output from the switch with the frequency modification module to create a frequency modified signal; and outputting the frequency modified signal.

In the same field of endeavor, Kapetanic et al. clearly disclose for each and every switch operation changing the modification of the frequency of the signal output from a switch with the frequency modification module to create a frequency modified signal; and outputting the frequency modified signal on a single output without the frequency modified signal passing through a switch as part of the outputting (figure 1, switch 10, frequency changer 96, column 6 line 65-column 7 line 18; when switch 10 switches, frequency modifiers 80 and 96 re-adjust themselves to achieve a new specific frequency, column 6 line 65-column 7 line 53, column 8 lines 15-43).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Kapetanic et al. into the art of Takenouchi et al. as to include controllable frequency modifying means for providing further dynamic frequency control.

Consider **claim 9 as applied to claim 8**, Takenouchi et al. as modified disclose wherein the first frequency and the second frequency are non-integer multiples. Such teaching is extremely well known in the art (**Lemay, US Patent (6321074)**, figure 2, non-integer multiplier 32, column 2 lines 37-45).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Lemay

into the art of Takenouchi et al. as modified as to include a non-integer multiplier for reducing harmonic cross coupling.

Consider **claim 10 as applied to claim 8**, Takenouchi et al. as modified disclose limiting processing comprises converting a sinusoidal type signal to a square wave signal.

Such converting method is extremely well known in the art (**Tahernia et al. (US Patent 4896122,** figure 3, column 5 lines 54-66).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Tahernia et al. into the art of Takenouchi et al. as modified as to include controllable frequency modifying means for providing further dynamic frequency control.

Consider **claim 11 as applied to claim 10**, Takenouchi et al. as modified disclose wherein the limiting function comprises converting a sinusoidal signal to a signal resembling a square wave signal.

Such converting method is extremely well known in the art (**Tahernia et al. (US Patent 4896122,** figure 3, column 5 lines 54-66).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Tahernia et al. into the art of Takenouchi et al. as modified as to include controllable frequency modifying means for providing further dynamic frequency control.

Consider **claim 12 as applied to claim 8**, Takenouchi et al. as modified disclose wherein the frequency modification module does not modify the frequency of both the

first signal and the second signal (it is optional to include the frequency modification module, the first or second frequency signal could be a specific frequency).

Consider **claim 13 as applied to claim 8**, Takenouchi et al. as modified disclose wherein the frequency modification module modifies the frequency of the first signal by an amount different than the amount of modification to the frequency of the second signal or a limit processed version of the second signal (Kapetanic et al., figure 1, switch 10, frequency changer 96, column 6 line 65-column 7 line 18).

Claims 14-18, 21 and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Takenouchi et al. (JP 06-338793)** in view of **Kapetanic et al. (US Patent 6163223)** and **Lemay, US Patent (6321074)**.

Consider **claim 14**, Takenouchi et al. clearly disclose a system for generating an output signal, wherein the output signal is capable of being switched between two or more output frequencies (drawing 1), the system comprising: two or more signal generators configured to generate two or more signals (drawing 1, PLL synthesizers 52 and 53), wherein each signal is at a different frequency (paragraph 22); a switch configured to receive at least two signals of the two or more signals and responsive to a control signal output a switch output comprising one of the two or more signals (drawing 1, SW 42 controlled by CPU 43).

However, Takenouchi et al. fail to disclose a frequency modification device configured to receive the switch output and modify the frequency of the switch output to a desired output frequency.

In the same field of endeavor, Kapetanic et al. clearly disclose a frequency modification device configured to receive the switch output after switching and modify the frequency of the switch output to a desired output frequency to create an output signal, wherein for every change in the switch output a frequency modification change also occurs, wherein an additional switch is not present after the frequency modification device (when switch 10 switches, frequency modifiers 80 and 96 re-adjust themselves to achieve a new specific frequency, column 6 line 65-column 7 line 53, column 8 lines 15-43; figure 1, switch 10, frequency changer 96, column 6 line 65-column 7 line 18).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Kapetanic et al. into the art of Takenouchi et al. as to include controllable frequency modifying means for providing further dynamic frequency control.

Takenouchi et al. fail to disclose one or more multiplier, dividers, or both configured to receive at least one of the two or more signals and process the at least one signal to create a first signal at a first frequency or a second signal at a second frequency such that the second frequency is a non-integer multiple of the first signal.

Lemay discloses (figure 2, non-integer multiplier 32, column 2 lines 37-45) "The output frequency is structured to be larger than the synthesizer VCO frequency by a rational (non-integer) factor greater than unity, thus maintaining a non-harmonic relationship between the output VCO and the synthesizer."

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Lemay

into the art of Takenouchi et al. as to include a non-integer multiplier to produce a second signal with a non-integer multiplies a first signal for reducing harmonic cross coupling.

Consider **claim 15 as applied to claim 14**, Takenouchi et al. as modified disclose wherein the two or more signal generators generate signals that are at frequencies that are non-integer multiples.

Such teaching is extremely well known in the art (Lemay, US Patent (6321074), figure 2, non-integer multiplier 32, column 2 lines 37-45).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Lemay into the art of Takenouchi et al. as modified as to include a non-integer multiplier for reducing harmonic cross coupling.

Consider **claim 16 as applied to claim 14**, Takenouchi et al. as modified disclose further comprising a controller configured to generate one or more control signals wherein the control signals synchronize switch output with frequency modification device operation and such synchronization forces a change in the frequency modification for every change in switch output (drawing 1, SW 42 and frequency changer 96 are controlled by CPU 43 as to output a specific frequency signal).

Consider **claim 17 as applied to claim 14**, Takenouchi et al. as modified disclose wherein the different frequencies of the two or more signals are selected to minimize cross-coupling between the two or more signals.

Such teaching is extremely well known in the art (Lemay, US Patent (6321074), figure 2, non-integer multiplier 32, column 2 lines 37-45).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Lemay into the art of Takenouchi et al. as modified as to produce a second signal with a non-integer multiplies a first signal for reducing harmonic cross coupling.

Consider **claim 18 as applied to claim 14**, Takenouchi et al. as modified disclose wherein the amount of frequency modification performed on a signal is directly proportional to the frequency of a signal and a desired output frequency (drawing 1, SW 42 and frequency changer 96 are controlled by CPU 43 as to output a specific frequency signal).

Consider **claim 21 as applied to claim 14**, Takenouchi et al. as modified disclose wherein the output signal is for use as a local oscillator signal in a wireless communication device (paragraphs 2 and 3).

Consider **claim 25 as applied to claim 22**, Takenouchi et al. as modified disclose wherein the first frequency and the second frequency are selected to reduce cross-coupling between signals and the system is embodied in an integrated circuit.

Such teaching is extremely well known in the art (Lemay, US Patent (6321074), figure 2, non-integer multiplier 32, column 2 lines 37-45).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Lemay

into the art of Takenouchi et al. as modified as to produce a second signal with a non-integer multiplies a first signal for reducing harmonic cross coupling.

Consider **claim 26 as applied to claim 22**, Takenouchi et al. as modified disclose wherein the ratio between the first frequency and the second frequency is a non-integer value.

Such teaching is extremely well known in the art (Lemay, US Patent (6321074), figure 2, non-integer multiplier 32, column 2 lines 37-45).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Lemay into the art of Takenouchi et al. as modified as to produce a second signal with a non-integer multiplies a first signal for reducing harmonic cross coupling.

Claims 22-23 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Takenouchi et al. (JP 06-338793)** in view of **Kapetanic et al. (US Patent 6163223).**

Consider **claim 22**, Takenouchi et al. clearly disclose a system for rapidly switching the frequency of an output signal between a first frequency and a second frequency comprising: a switch configured to receive a first signal at a first frequency and a second signal at a second frequency and responsive to a control signal output either of the first signal or the second signal (drawing 1, SW42 controlled by CPU 43 as to output a frequency signal).

However, Takenouchi et al. fail to disclose a frequency modification device configured to, responsive to a control signal, increase or decrease the frequency of a signal output from the switch to either the third frequency or the fourth frequency.

In the same field of endeavor, Kapetanic et al. clearly disclose a plurality of frequency generators 2 and 4 (figure 1) which outputting two different frequency signals to switch 10, a frequency modification device 96 configured to, responsive to a control signal, increase or decrease the frequency of a signal output from the switch to either the third frequency or the fourth frequency wherein for every change in switch output, an increase or decrease in the frequency of a signal output from the switch occurs to create a frequency modified signal, an output configured to output the frequency modified signal such that a switch is not located between the frequency modification device and the output (figure 1, switch 10, frequency changer 96, column 6 line 65-column 7 line 18; when switch 10 switches, frequency modifiers 80 and 96 re-adjust themselves to achieve a new specific frequency, column 6 line 65-column 7 line 53, column 8 lines 15-43), wherein switch 10 and switches 104 and 106 are synchronized so as to provide a desire frequency output signal.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Kapetanic et al. into the art of Takenouchi et al. as to include controllable frequency modifying means for providing further dynamic frequency control, thus a controller (CPU 43) configured to control SW 42 and frequency changer 96 to provide to thereby

synchronize which signal is output from the switch 42 with frequency modification device operation 96.

Consider **claim 23 as applied to claim 22**, Takenouchi et al. as modified disclose wherein the frequency modification device comprises a frequency multiplier configured to multiply a received signal by a value necessary to modify the frequency of the received signal to either the third frequency or the fourth frequency (Kapetanic et al., figure 1, switch 10, frequency changer 96, column 6 line 65-column 7 line 18).

Consider **claim 27 as applied to claim 22**, Takenouchi et al. as modified disclose further comprising at least one signal generator (drawing 1, PLL synthesizer 52) configured to generate the first signal, and wherein the controller (drawing 1, paragraph 22, CPU controls the first and the second PLLs 32 and 33 to generate the first and the second frequency signals) is further configured to provide a control signal to at least one signal generator to control which frequency is generated.

Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Takenouchi et al. (JP 06-338793)** as modified by **Kapetanic et al. (US Patent 6163223) and Lemay, US Patent (6321074)** in view of **Hjipieris et al. (US Patent 5237291).**

Consider **claim 19 as applied to claim 14**, Takenouchi et al. as modified fail to disclose further comprising a limiter configured to modify the two or more signals prior to switching to reduce cross-coupling between the two or more signals within the switch.

In the same field of endeavor, Hjipieris et al. disclose filters for removing unwanted harmonics from a generated oscillating signal wherein processing the first signal to reduce harmonic cross-coupling thereby creating a processed first signal; and processing the second signal to reduce harmonic cross-coupling thereby creating a processed second signal (figure 1, filters 17, 15 and 13, column 2 lines 27-40).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Hjipieris et al. into the art of Takenouchi et al. as modified as to include the filters for removing unwanted harmonic cross coupling.

Consider **claim 20 as applied to claim 19**, Takenouchi et al. as modified disclose wherein two or more signals generated by the two or more signal generators comprise non-square wave signals (drawing 1, a reference signal oscillator 31).

However, Takenouchi et al. as modified fail to disclose the limiter converts a signal to format more closely approaching a square wave signal.

Such converting method is extremely well known in the art (**Tahernia et al. (US Patent 4896122,** figure 3, column 5 lines 54-66).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Tahernia et al. into the art of Takenouchi et al. as modified as to include controllable frequency modifying means for providing further dynamic frequency control.

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Takenouchi et al. (JP 06-338793)** as modified by **Kapetanic et al. (US Patent 6163223)** in view of **Hjipieris et al. (US Patent 5237291).**

Consider **claim 24 as applied to claim 22**, Takenouchi et al. as modified fail to disclose further comprising one or more limiters configured to modify at least one input to the switch to thereby reduce cross-coupling between the first signal and the second signal.

In the same field of endeavor, Hjipieris et al. disclose filters for removing unwanted harmonics from a generated oscillating signal wherein processing the first signal to reduce harmonic cross-coupling thereby creating a processed first signal; and processing the second signal to reduce harmonic cross-coupling thereby creating a processed second signal (figure 1, filters 17, 15 and 13, column 2 lines 27-40).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Hjipieris et al. into the art of Takenouchi et al. as modified as to include the filters for removing unwanted harmonic cross coupling.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to:**

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to RuiMeng Hu whose telephone number is 571-270-1105. The examiner can normally be reached on Monday - Thursday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on 571-272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/RuiMeng Hu/
R.H./rh
August 18, 2009

/Lana N. Le/
Primary Examiner, Art Unit 2614